Low-Power Design of a 64-tap, 4-bit Digital Matched Filter using Systolic Array Architecture and CVSL Circuit Techniques in CMOS

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Abstract

A 4-bit 64-chip Pseudo Noise (PN) coded Digital Matched Filter (DMF) is designed in 0.7um CMOS technology using Systolic Array (SA) architecture. Full-custom and full-static Cascode Voltage Switch Logic (CVSL) circuit techniques have been employed in the implementation of the basic building blocks (systoles) of the SA DMF. Significant reduction in number of transistors and power consumption have been achieved. The resultant IC is to be used at the receiver side of a wireless Direct Sequence Spread Spectrum (DSSS) communication system.

1. Introduction

Digital Matched Filters are used for instantaneous PN-code acquisition at the receiver side of DSSS systems. A DMF performs convolution of the time-reversed replica of the PN-code with the incoming signal (despreading) [1] and has an impulse response as given in the following formula:

$$v_{i/q,k} = \sum_{n=1}^{L-1} S_{L-n} w_{i/q,k-n}$$

L: PN-code length
v: convolution result at time k
S: PN-code coefficient
w: matched filter input data
i/q: in/quadrature phase

Matched Filters are realized in baseband after the incoming signal is down-converted by quadrature carriers. So the DMF contains two quadrature correlators using the same PN-code and samples incoming digitized data at Nyquist rate. By employing a moving average filter with a window size of two samples at the filter inputs, the average of two consecutive inputs are fed into the DMF, hence the convolution can be reduced to the following form for the sake of architectural simplicity:

$$v_{i/q,k} = \sum_{n=1}^{L-1} S_{L-n} w_{i/q,k-(2n+1)}$$

The outputs of two quadrature correlators are fed into a square-law envelope detector to calculate the magnitude of the filtered signal. Robertson's "Fast Amplitude Approximation Formula [2] is used to realize the envelope detector:

$$y_{ek} = \sqrt{v_{ik}^2 + v_{qk}^2} \approx max\left\{|v_{ik}|,|v_{qk}|\right\} + \frac{1}{2} \times min\left\{|v_{ik}|,|v_{qk}|\right\}$$

For wireless communication applications, where low power design is mandatory, digital implementation of matched filters in CMOS is efficient. In this study, a DMF, consisting of dual correlators, averagers and an envelope detector, is designed to despread 64-chip PN-coded signals of 4-bit input length. Each PN-code takes on values {+1,-1} and represented by a single bit. An operating frequency of 64MHz at 3V supply voltage is aimed in a temperature range of -40C - +85C.

Systolic Array architecture is preferred for design reusability and modularity.

2. Systolic Array Architecture

A systolic system is an array of processors where all data, while being shifted regularly across the array, can be used in all processing elements.[3]

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Table 1. 4-Tap Systolic DMF data flow

INPUTS	OUTPUTS			
w_i	y_1	y_2	y_3	y_4
w_1	S_1w_1	S_2w_1	S_3w_1	S_4w_1
w_2	S_1w_2	$S_2w_2+S_1w_1$	$S_3w_2+S_2w_1$	$S_4w_2+S_3w_1$
w_3	S_1w_3	$S_2w_3+S_1w_2$	$S_3w_3+S_2w_2+S_1w_1$	$S_4w_3+S_3w_2+S_2w_1$
w_4	S_1w_4	$S_2w_4+S_1w_3$	$S_3w_4+S_2w_3+S_1w_2$	$\underbrace{S_4w_4+S_3w_3+S_2w_2+S_1w_1}_{acquisition}$
w_5	S_1w_5	$S_2w_5+S_1w_4$	$S_3w_5+S_2w_4+S_1w_3$	$S_4w_5+S_3w_4+S_2w_3+S_1w_2$

Systolic arrays are constructed by replicating a processing element (Systole), so design task is reduced to partitioning the operation into identical tasks that follow each other in a coherent fashion [4]. For convolution operation, the task of each systole is to multiply its input with the corresponding PN-code coefficient and add the result to the sum contributed by the previous systole (Figure 1).

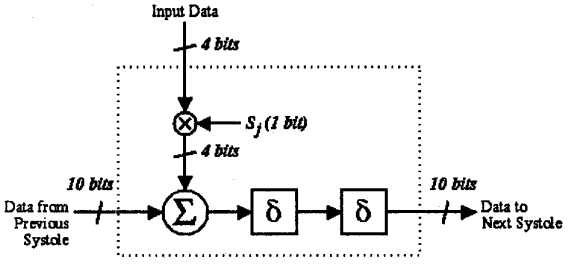

Figure 1. Systole for DMF

A Systolic Array DMF produces output with zero latency as seen in Figure 2 and in Table 1.

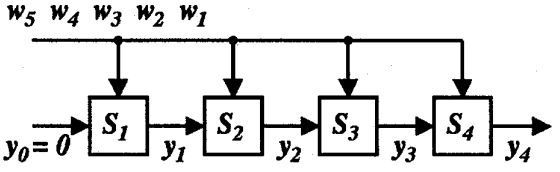

Figure 2. Sample 4-Tap Systolic DMF

Since PN-codes are 1-bit in this study, the multiplication operation is reduced to a sign change operation (EX-OR) so the complexity of each systole is determined chiefly by the adder block which also determines the maximum operating frequency of DMF.

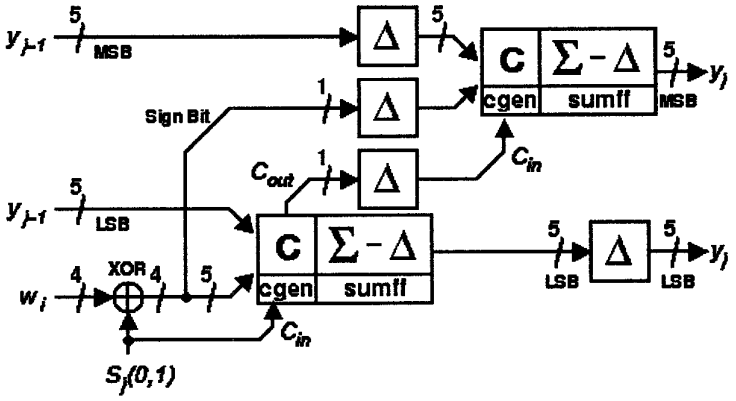

Figure 3. Architecture of a Systole

3. Systolic Array DMF Implementation

3.1. Systole Design

The SA DMF accepts 4-bit inputs and produces 10-bit filtered outputs after performing convolution in 64-taps. Therefore each systole in SA contributes its processed data to the 10-bit data stream. The operating frequency of a systole is bounded by the speed of the 10-bit multiply (ex-or)-and-add block. To meet the speed requirement, the 10-bit addition is divided into two 5-bit additions by using the second delay element in the systole architecture like a pipe-lining stage. Thus no additional latency is introduced (Figure 3).

To take full advantage of systolic array architectures, full-custom design methods are employed in systole design.

3.2. CVSL Design of Basic Building Blocks

In order to meet low power and high speed constraints in small silicon area, while maintaining static operation, several forms of CVSL logic are utilized in the basic building blocks of a systole.

Single-transistor-clocked differential CVSL flip-flop proposed in [5] by Yuan and Svensson is optimized for 0.7um technology and used as the delay element in systoles (Figure 4). Using only two clocked transistors in each flip-flop, not only a significant power saving (90%) is achieved, but also design of the clock buffer for the SA DMF core is simplified considerably.

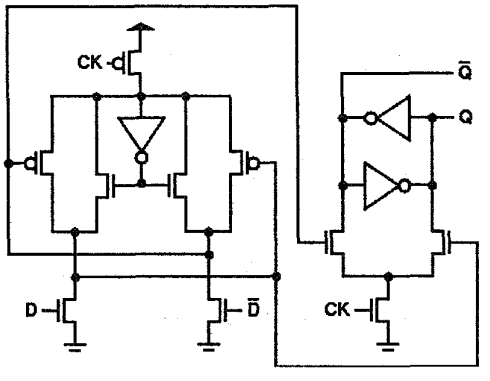

Figure 4. Differential CVSL Flip-flop

The 5-bit adders are realized as ripple carry adders where the sum generating logic is embedded into the p-stage of CVSL flip-flops to optimize area and power (Figure 5). This way, the effective power consumed by a summing block is reduced by 75% with respect to the standard cells in 0.7um library.

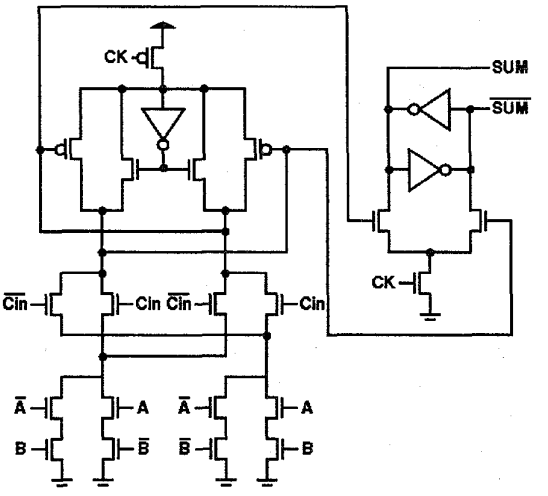

Figure 5. Summing CVSL Flip-flop

The carry-generating logic of adders and the multiplication blocks (ex-or) are implemented using Differential CVSL with Pass-Gate (DCVSPG) Logic proposed by Lai and Hwang [6] (Figures 6 and 7). This circuit topology introduced a power saving of 90%.

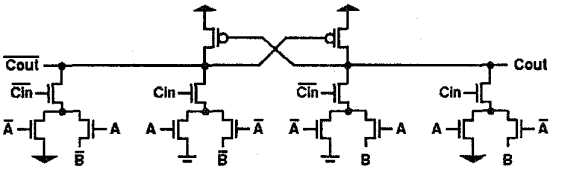

Figure 6. DCVSPG Carry-Generating Block

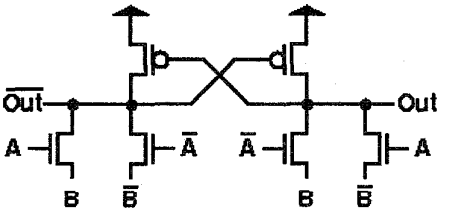

Figure 7. DCVSPG Ex-or

The last bit of the carry generating logic is also merged into the p-stage of CVSL flip-flops circuitry (Figure 8). Hence power consumption is reduced by 80%.

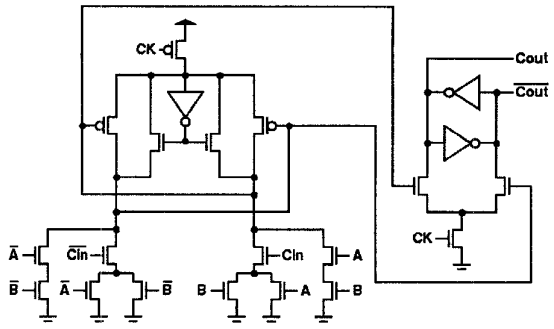

Figure 8. Carry-Generating CVSL Flip-flop

3.3. Layout Considerations

Since Systolic array is full custom, no interconnection problems are encountered in layout. The crucial point of SA DMF layout is keeping clock synchronization and avoiding clock skew which is maintained by applying the clock signal in the opposite direction to the data flow.

3.4. Simulations

The physical simulation results of the SA DMF are compared to the behavioral Matlab model of the system for functional verification [7].

Each full-custom designed CVSL block is simulated using analog simulator and its power consumption is measured for worst case operating conditions. These power consumption figures are compared to those of standard cells in the target technology and relative power reduction is calculated for each cell. A final analog worst case simulation is run on the complete custom-designed systole to observe total system performance.

4. Performance

The main characteristics of the resultant SA DMF IC is as presented in Table 2:

Table 2. Characteristics of SA DMF

Technology	0.7 μm
DMF Area / Channel	11.3 mm^2
Total Core Area	23.8 mm^2
Supply Voltage	2.7 - 5.5 V
Temperature Range	-40 - +85 °C
Operating Frequency	64 MHz Worst Case
Power Dissipation	350 mW Worst Case
Latency	0

5. Conclusions

Application of Systolic Array architecture in the design of DMF reduced the system design to design of a single systole and thus improved the design time and reusability of the design considerably. Besides, the resultant DMF architecture can be easily up-scalable for despreading longer PN-codes without introducing latency to the system.

Employing full-custom design methodology in systole design and utilization of alternative static CMOS circuit topologies like differential CVSL logic and CVSL with pass-transistor logic resulted in a huge amount of decrease (75%-90%) in power consumption without loss of speed as compared to conventional standard cell designs of the same feature size.

These characteristics make the SA DMF IC very suitable for low-power and high-speed wireless and mobile communication applications.

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