A Low-Power System-on-Chip for Telecommunications : Single Chip Digital FM Receiver/Demodulator IP

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Abstract

A single chip digital FM receiver/demodulator system, utilizing the zero-cross detection technique, is designed and implemented as an Intellectual Property (IP). Zero-cross detection is performed at an IF frequency of 10.7 MHz using a sampling clock of 65536 KHz. The system is simulated for BT=0.3 GMSK input with a data rate of 8000 bps. Simulations showed that the system has a performance comparable to those of ideal non-coherent FM demodulators [1]. Power dissipation and area of the system are also calculated for a 0.5 μm triple-metal standard digital CMOS process. It has been shown that the system would have a power dissipation very close to its analog counterparts when implemented with standard cells. For the case that custom flip-flop and adder cells such as ones given in [2] are used, digital implementation would draw much lower current than widely available analog circuits. The silicon area occupied by the system would be in the order of 3 mm², making it low cost. The designed system can be used as a single IC or as an IP in a larger IC, in low-cost mobile communication applications where non-coherent detection of the transmitted signal is desired.

1. Introduction

Frequency modulation has been the primary technique in wireless communication since 1930's [3]. FM demodulators are basic building blocks of low-cost mobile communication systems where non-coherent detection of the transmitted signal is desired.

Most of the conventional FM discriminator / demodulator architectures use quadrature detectors requiring bulky external components which have temperature and device-dependent gain. Another commonly used architecture is the PLL demodulator with additional IF-to-baseband downconversion circuitry. PLL demodulators are neither favourable due to their high power consumption [4]. In today's mobile communication systems, low-power consumption, low device costs and small device sizes are as important as signal quality and efficient usage of bandwidth.

With the recent advances in digital IC technology, alternative FM discriminator/demodulator techniques and fully integrated circuit structures, which are capable of satisfying these requirements, have begun to appear [4], [5].

The system presented in this study, is a modified and enhanced form of the digital FM demodulator in [5].

2. Zero-Cross Detection of FM

The zero-cross detection technique is based on counting the zero-crosses of a frequency modulated signal at IF, in order to convert the frequency variations into voltage levels. Each detected zero-cross is represented by a pulse and then these pulses are filtered by a narrowband low-pass filter. The output of the filter is the demodulated baseband signal with a DC-offset, where the DC-offset value represents the voltage level corresponding to the IF center frequency. When this offset is removed from the baseband signal, the transmitted signal is recovered [6].

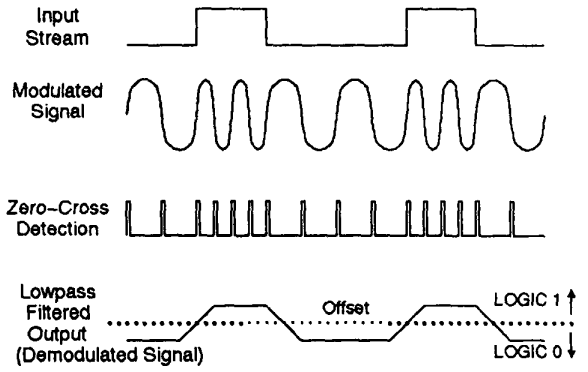

Figure 1. Zero Cross Detection of an FSK/MSK

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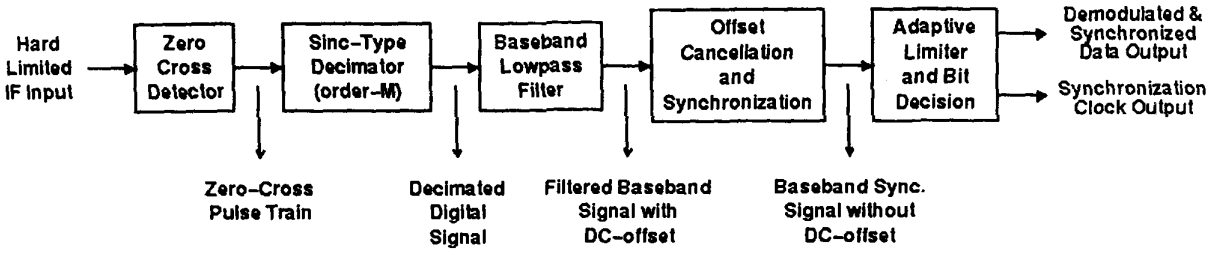

Figure 2. Block Diagram of Digital FM Discriminator/Demodulator

Signal

Variations in the IF center frequency, due to channel effects, will result in shifts from the expected DC-offset level. Offset compansation techniques should be employed to remove the actual DC-offset from the baseband signal for correct recovery of the transmitted signal against imperfections [7].

3. Construction of Digital FM Discriminator / Demodulator

The zero-cross detection technique realized in this study is the enhanced digital analogy (Figure 1) [8] of the very well-known analog implementation.

The incoming analog IF signal is first externally hard-limited and amplified to provide suitable digital signal levels. This signal is then sampled at a frequency which is orders of magnitude (usually 5-10) of the IF center frequency. Zero-crosses of the sampled IF signal are detected by logical EX-ORing each new sample with the previous one. The EX-OR gate generates a logic '1' pulse for each detected zero-cross. These pulses are then fed into a digital low-pass filter bank.

For easy and power and area-efficient implementation, a two stage sinc-cube decimation filter structure is used for low-pass filtering. The first sinc-cube filter, which has a relatively low decimation rate, performs wide-band filtering and down-conversion to an intermidiate digital operating frequency. Since the operating frequency of this stage is very high, the power consumption of the whole system is heavily determined at this stage. Hence selection of the decimation rate of this stage is a very critical point for the whole system. The decimation rate of this stage should be kept high enough to provide a low operating frequency at the second stage, and low enough to minimize the circuitry operating at the high frequency. The decimation rate of the first stage of the system presented in this study is chosen as 8.

In the second stage of sinc-cube decimation the signal is very narrowly low-pass filtered and down-converted to a rate which is 4 times the original data rate. The output of this stage is the demodulated baseband signal with DC-offset. Hence the two stage sinc-cube decimation structure acts as the FM discriminator.

In order to eliminate the noise furthermore, an additional low-pass filter is included at baseband, prior to offset cancellation. This filter would have negligible effect on the total power consumption due to its extremely low operating frequency and still less on total cost of the system. However it would serve to improve the BER performance considerably.

Offset cancellation is adaptively performed in two steps (Figure 3): At the first stage, a constant DC value corresponding to the selected IF center frequency is subtracted from the baseband signal. At the second stage, the variations in the IF center frequency due to channel conditions is detected using the preamble bits in the transmitted data, and the corresponding constant DC-value is removed from the output of the first stage.

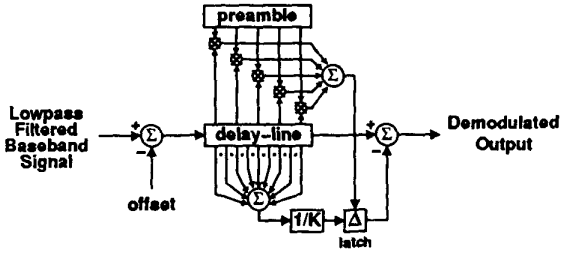

Figure 3. Block Diagram of Offset Cancellation and Synchronization Module

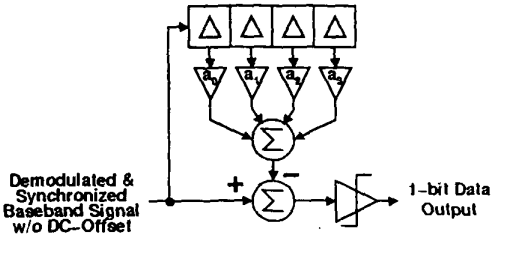

Figure 4. Block Diagram of Adaptive Limiter and Bit Decision Module

Preamble bits are detected using a correlator and a moving average filter, with a window size equal to the preamble frame size, continuously generating the arithmetical mean of the data in the window. Upon each preamble detection, output of the moving average filter is latched as the actual DC-offset value to be removed from the baseband signal. The preamble detection scheme also provides a reference for data clock at the actual data rate.

After offset cancellation, the signal is applied to an adaptive limiter for bit decision: The adaptive limiter (Figure 4) calculates the weighted average of the last 4 samples, corresponding to a bit duration, and subtracts this value from the latest sample. This operation prevents wrong detection of single bit changes in the incoming data due to Gaussian pulse shaping in GFSK and GMSK modulations. The data at the output of the adaptive limiter is down-sampled to its original rate by the extracted data clock [5]. Thus the synchronized data output and receiver clock are generated by the digital FM demodulator.

The constructed FM discriminator / demodulator is implemented as programmable for different data rates and frequency modulation schemes such as FSK, GFSK, MSK and GMSK.

4. Performance Measurements

The performance of the presented FM discriminator / demodulator is evaluated by applying a GMSK simulation input with BT=0.3 and 8000 bps data rate at an IF center frequency of 10.7 MHz and a sampling frequency of 65536 KHz. White-gaussian noise, at various levels, is added to the input IF signal; and bit-error rate (BER) is measured at the baseband output for each noise level. The resultant BER performance curve against SNR of the proposed system is sketched in Figure 5. The BER vs SNR curves of an ideal non-coherent demodulator [1] and Viterbi-4 demodulator [9] as an optimum receiver are also included in this figure for the sake of comparison.

As seen in Figure 5, the Digital FM demodulator / discriminator circuit shows a performance which is comparable to an ideal non-coherent demodulator and slightly better for low SNR values.

The BER performance of the digital FM demodulator / discriminator was also measured against frequency variations of ± 100 Hz at the IF center frequency and displayed very close results to the case with no deviation from the carrier frequency. This validates the operation of the offset cancellation scheme applied in this architecture.

In order to see the effects of power reduction techniques, the demodulator IP was also simulated for half the sampling frequency (32768 KHz), and the resultant BER vs. SNR curve is sketched in Figure 5. In this configuration, SNR performance was reduced by 2.5 dB, while power consumption was reduced by 75%. This simulation also validated the reconfigurability of the Digital FM Demodulator IP.

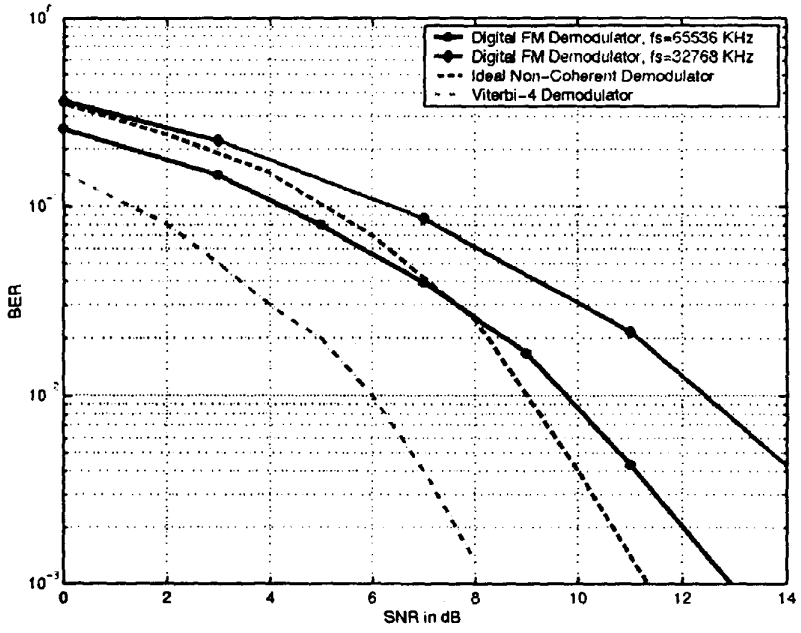

Figure 5. BER vs SNR Curves

5. Results and Conclusions

The zero-cross detection scheme utilized in the proposed Digital FM discriminator / demodulator architecture attained a BER vs SNR performance which is comparable to conventional non-coherent FM demodulation schemes. The BER performance further increases at low SNR values, making this system especially advantageous for noisy channels or low power transmission. The system also displays a stable performance against variations in the carrier frequency without employing a PLL circuitry.

The presented FM discriminator / demodulator circuit is implemented as a soft IP and its power and area figures are analyzed for a 0.5 μm triple-metal standard digital CMOS process. With an operating supply voltage of 3 Volts, the total current consumption will be around 1.5 mA at an IF sampling frequency of 65536 KHz. The current drawn by the system will drop down to 0.5 mA, if custom flip-flop and adder cells utilizing the circuit structures in [2] are used instead of standard cells. Total core area will be around 3 mm^2, for both cases. When implemented using standard cells, the IP will be independent of technology and can be remapped to any cell library.

The designed FM discriminator/demodulator IP takes full advantage of digital design techniques providing a highly integrated solution on a single chip, without requiring an A/D converter, analog circuitry or external components.

As a result, a satisfactory BER performance is attained at low power and low cost, while providing reliable operation against temperature and device-dependent parameters. If still lower power consumption is required, the operating frequency of the IP can be decreased at the expense of BER performance.

6. References

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