DESIGN OF A FULLY-STATIC DIFFERENTIAL LOW-POWER CMOS FLIP-FLOP

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ABSTRACT

A fully-static flip-flop structure is proposed and compared to both the conventional CMOS flip-flop and the Cascode Voltage Switch Logic (CVSL) static flip-flop proposed by Yuan and Svensson [1], in terms of speed, power consumption and silicon area. Then an add-and-delay circuit is implemented using all three flip-flop structures to demonstrate the performance of the proposed flip-flop. The add-and-delay structure is chosen since it is a widely used block in digital signal processing. The proposed structure showed to be consuming less power and occupying smaller silicon area. It has the additional advantage of being easier to merge with pass-transistor logic structures.

1. INTRODUCTION

Delay elements are basic building blocks for CMOS digital chips [2]. For digital implementation, foundries and/or design houses prepare standard cell libraries for each technology they develop. These libraries employ the very well known CMOS-switch and inverter based flip-flops [3], as the delay elements. The conventional switch and inverter based flip-flops, while providing a very stable and easy-to-implement structure, suffer form the lack of flexibility. Extra logic and functionality can not be easily embedded into such structures. They also consume relatively high power compared to other cells in the library and have several clocked transistors, therefore always making clock-distribution a hard-to-solve problem.

In this study, a new fully-static flip-flop structure is proposed, and compared to the conventional static CMOS flip-flop and the fully-static CVSL flip-flop proposed by Yuan and Svensson in (Figure 1). An add-and-delay circuit, which is a basic building block for most digital signal processing applications, is built using this new flip-flop with Differential Cascode Voltage Switch with Pass-Gate (DCVSPG) techniques [4] and compared to a similar circuit implemented with Yuan's CVSL flip-flop. 0.7μm digital CMOS technology is used in all implementations.

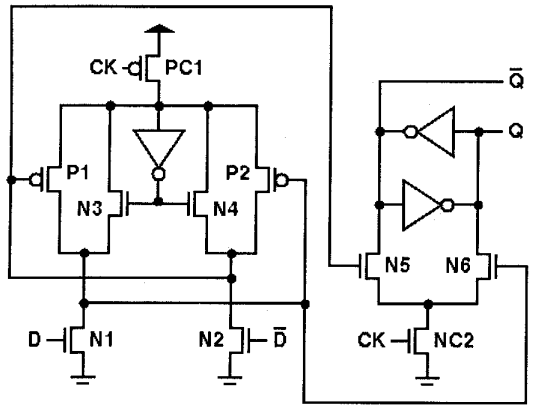

Figure 1. Yuan and Svensson's CVSL Flip-flop.

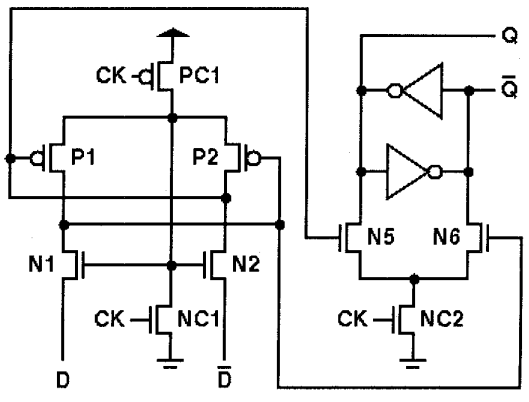

Figure 2. New CVSL Flip-flop.

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Table 1. Delay and Power Characteristics of the Two Flip-flops

	Fan-Out				
	0	**1**	**2**	**4**	**8**
Yuan and Svensson's CVSL Flip-Flop					
Delay @ 100 MHz	2.08 ns	2.20 ns	2.29 ns	2.47 ns	2.92 ns
Delay @ 10 MHz	2.10 ns	2.21 ns	2.32 ns	2.52 ns	2.93 ns
Delay @ 1 MHz	2.11 ns	2.21 ns	2.33 ns	2.55 ns	2.94 ns
Power @ 100 MHz (μW/MHz)	2.06	3.90	6.44	10.36	17.70
Power @ 10 MHz (μW/MHz)	4.56	9.21	13.35	21.04	33.20
Power @ 1 MHz (μW/MHz)	4.47	9.06	13.38	21.19	33.6
The New CVSL Flip-Flop					
Delay @ 100 MHz	2.25 ns	2.38 ns	2.55 ns	2.85 ns	3.25 ns
Delay @ 10 MHz	2.27 ns	2.47 ns	2.63 ns	2.95 ns	3.50 ns
Delay @ 1 MHz	2.28 ns	2.48 ns	2.67 ns	2.99 ns	3.56 ns
Power @ 100 MHz (μW/MHz)	2.12	4.26	6.36	10.36	14.71
Power @ 10 MHz (μW/MHz)	2.10	3.77	6.29	11.00	20.05
Power @ 1 MHz (μW/MHz)	2.17	4.38	6.70	11.78	19.19

2. NEW STATIC CVSL FLIP-FLOP

The circuit schematic of the proposed static CVSL flip-flop is given in Figure 2. This flip-flop structure is obtained by modifying the first (p) stage of Yuan and Svensson's flip-flop as follows: A third clocked transistor (NC1) is added to the first stage, while the inverter and N3-N4 transistors, used to keep the internal nodes of the flip-flop at zero potential, are eliminated. The remaining N1-N2 transistors at the input stage are modified as clock controlled n-type pass transistors. This way, no floating nodes are left to be pulled up by the P1-P2 transistors when clock is at its zero-state. Instead, one of the P1-P2 transistors has to strengthen a weak logic-one passed by the corresponding N1 or N2 transistor, while the other p-transistor is kept off by the logic-one at its gate. During the transition of clock from zero to one, the differential state of the first stage is transferred to the second stage. Then the N1-N2 transistors isolate the internal nodes from the inputs and pull all these internal nodes to logic-zero. Due to the imperfect zero-transmission nature of p-transistors, one of the output nodes of the first stage can only be pulled to weak zero. Still this potential is enough to keep the N5-N6 transistors off; and the back-to-back connected inverters keep the new logic-state until the next zero-to-one transition of the clock.

Yuan and Svensson's flip-flop and the new CVSL flip-flop are simulated for different load and operating conditions using the Spice parameters of a 0.7 μm digital CMOS technology. Simulation results for both flip-flops are given in Table 1. As seen in the table, the delay characteristics for both flip-flops are comparable, while the new CVSL flip-flop shows a uniform and lower power consumption characteristics with respect to load and frequency.

The proposed CVSL flip-flop is advantageous also in terms of silicon area and number of transistors used, since it uses only 11 transistors, whereas the number of transistors in Yuan's flip-flop is 14 and that of a conventional structure is 18.

3. ADD-AND-DELAY CIRCUITS

Since add-and-delay blocks are extensively used in digital signal processing applications, efficient implementation of such blocks is a major application

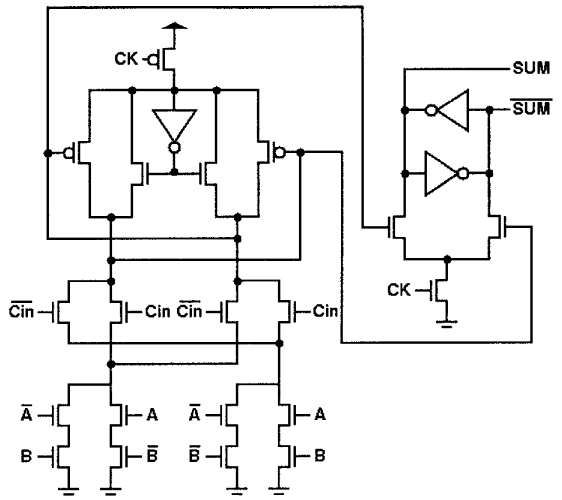

Figure 3. Add-and-Delay Circuit using the New CVSL Flip-flop and DCVSPG technique

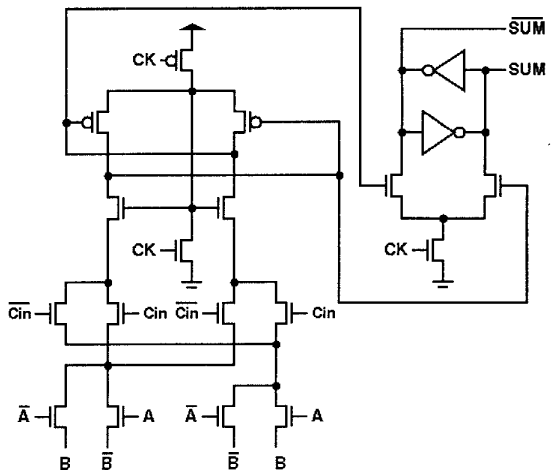

Figure 4. Add-and-Delay Circuit using the Yuan and Svensson's CVSL Flip-flop.

problem. Two add-and-delay blocks are designed and implemented using both the proposed flip-flop with DCVSPG logic structures (DCVSPG-AAD) and Yuan's flip-flop with CVSL structures (CVSL-AAD). The resultant circuit schematics are given in Figures 3 and 4.

The two add-and-delay circuits are simulated for different load and operating conditions using the Spice parameters of a 0.7 μm digital CMOS technology. Simulation results for both circuits are given in Table 2. As seen in the table, the power consumption for both circuits are comparable while the circuit implemented using the new CVLS flip-flop is faster and occupies smaller area using less number of transistors.

Table 2. Comparison of the Two Add-and-Delay Circuits

	CVSL Add-and-Delay	New CVSL Add-and-Delay
Max. Operating Frequency	166 MHz	177 Mhz
Power Dissipation @ 100 MHz	< 225 μW	< 240 μW
# of Transistors	30	25
# of Clocked Transistors	2	3
Block Area	0.28 mm^2	0.23 mm^2

4. CONCLUSIONS

We have modified the static CVSL flip-flop proposed by Yuan and Svensson in order to obtain a new CVSL flip-flop with lower power consumption and smaller area. The new CVSL flip-flop is suitable for both full-custom designs and standard cell libraries, since it is fully-static. Pass-transistor and standard CMOS logic can be merged to the input stage of the new CVSL flip-flop, providing flexibility for faster circuit implementations in smaller silicon area.

5. REFERENCES

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