

LOW-POWER DESIGN OF A DIGITAL FM DEMODULATOR BASED ON ZERO-CROSS DETECTION AT IF

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ABSTRACT

A digital FM receiver/demodulator system, utilizing the zero-cross detection technique [1], is designed and implemented on a single IC. Zero-cross detection is performed at an IF frequency of 455 kHz. The system is simulated for $BT=0.3$ GMSK input with an input data rate of 8000 bps and displayed a better BER Performance than coherent detectors. The developed system is implemented in $0.5 \mu\text{m}$ triple-metal standard digital CMOS technology. Power dissipation of the resultant IC is less than its analog counterparts while the occupied silicon area is very small making it low cost. The FM receiver/demodulator IC is suitable to be used in low-power and low-cost mobile communication applications providing better BER performance than conventional systems, especially in noisy channels.

1. INTRODUCTION

Frequency modulation has been the primary technique in wireless communication since 1930's [2]. FM demodulators are basic building blocks of low-cost mobile communication systems where non-coherent detection of the transmitted signal is desired.

The conventional FM discriminator/demodulator architectures use either quadrature detectors or PLL demodulators with additional IF-to-baseband downconversion circuitry. Quadrature detectors require bulky external components which have temperature and device-dependent gain. PLL demodulators are neither favorable due to their high power consumption [3].

However, in mobile telecommunications, low-power consumption, low device costs and small device sizes are as important as signal quality and efficient usage of bandwidth. To satisfy these requirements, alternative FM discriminator/demodulator structures and fully

integrated circuit techniques should be employed.

In this study, the zero-cross detection technique for FM discrimination/demodulation has been digitally utilized and implemented in CMOS on a single IC. Power consumption and design complexity have been considerably reduced using digital design techniques in addition to the advantages of reliability, scalability and cost-effectiveness of digital CMOS circuits.

2. ZERO-CROSS DETECTION FOR FM DISCRIMINATION

The zero-cross detection technique is based on counting the zero-crosses of a frequency modulated signal at IF, in order to convert the frequency variations into voltage levels [1]. Each detected zero-cross is represented by a pulse and then these pulses are filtered by a narrowband low-pass filter (Figure 1). The output of the filter is the demodulated baseband signal with a DC-offset, where the DC-offset value represents the voltage level corresponding to the IF center frequency. When this offset is removed from the baseband signal, the transmitted signal is recovered [4].

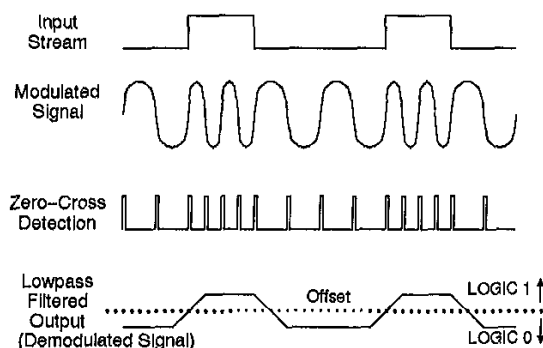


Figure 1. Zero Cross Detection of an FSK/MSK Signal

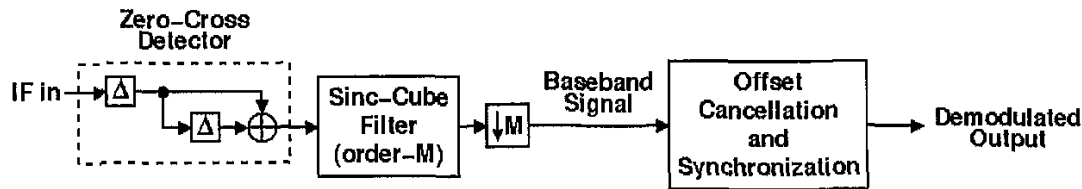


Figure 2. Block Diagram of Digital FM Discriminator/Demodulator

Variations in the IF center frequency, due to imperfections, will result in shifts from the expected DC-offset level. Offset cancellation techniques should be employed to remove the actual DC-offset from the baseband signal for correct recovery of the transmitted signal against imperfections [5].

3. CONSTRUCTION OF DIGITAL FM DISCRIMINATOR/DEMOMULATOR

The zero-cross detection technique, which is conventionally implemented in analog, can be easily realized in digital (Figure 2) [1]:

The incoming analog IF signal, which is externally hard-limited to provide suitable digital signal levels, is sampled at a frequency which is sufficiently higher than the IF center frequency, for digital processing. The zero-cross detection is achieved by performing the logical ex-or operation of each sample with the previous sample. The output of the ex-or gate is a logic '1' pulse when a zero-cross is detected. These pulses are then fed into a digital low-pass filter.

For easy and area-efficient implementation, a sinc-cube decimation filter is used as low-pass filter. The sinc-cube filter, having a high decimation rate, performs narrow-band filtering and down-conversion to baseband frequency of the incoming signal. At the output of sinc-cube decimation filter, demodulated baseband signal with DC-offset is obtained at 4 times the data rate.

Offset cancellation is adaptively performed in two steps (Figure 3): At the first stage, a constant DC value corresponding to the selected IF center frequency is subtracted from the baseband signal. At the second stage, the deviations in the IF center frequency due to channel conditions is calculated using the preamble bits in the transmitted data, and the corresponding constant DC-value is removed from the output of the first stage. Preamble bits are detected using a correlator and a moving average filter, with a window size equal to the preamble frame size, continuously generating the arithmetical mean of the data in the window. Upon each preamble detection, output of the moving average filter is latched as the

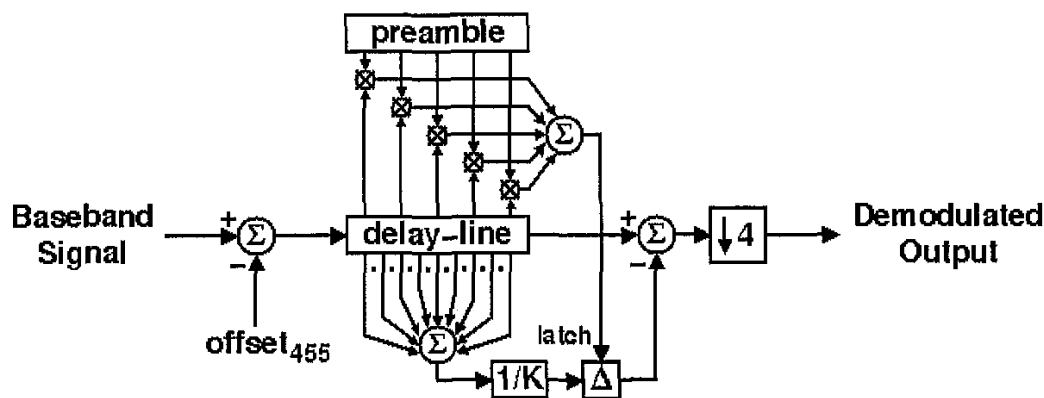


Figure 3. Block Diagram of Offset Cancellation and Synchronization Module

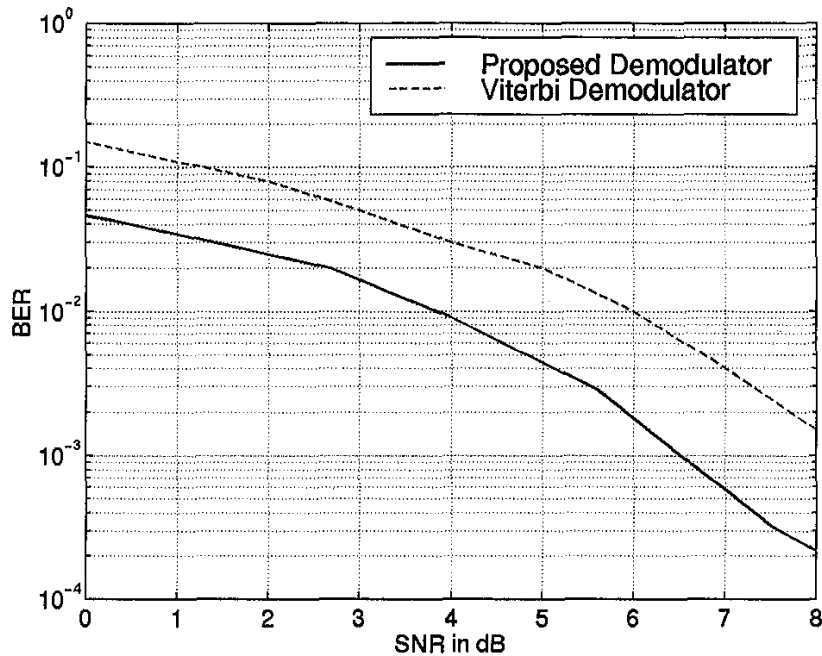


Figure 4. BER vs SNR Curves

actual DC-offset value to be removed from the baseband signal. The preamble detection scheme also provides a reference for receiver clock at 4 times the actual data rate and synchronization to incoming data is achieved as well. Then, using the synchronized receiver clock, data is down-sampled to its original rate by taking every second sample out of the 4 samples of a data symbol.

The constructed FM discriminator/demodulator is implemented as programmable for different data rates and frequency modulation schemes such as FSK, GFSK, MSK and GMSK.

4. PERFORMANCE MEASUREMENTS

For performance measurements, the presented FM discriminator/demodulator is simulated with a $BT=0.3$ GMSK modulated signal at 8000 bps data rate and 455 KHz IF center frequency. For the evaluation of noise performance, white-gaussian baseband noise, at different levels, is added to the input signal; and bit-error rate is measured at the baseband output for each noise level. The resultant BER performance curve against SNR of the proposed system is sketched in Figure 4. The

BER vs SNR curve of a Viterbi demodulator [6] is also included in this figure for the sake of comparison.

As seen in Figure 4, the Digital FM Demodulator/discriminator circuit shows a performance which is 2-2.5 dB better than a Viterbi demodulator. Especially for low SNR levels, the Digital FM Demodulator/discriminator achieves better BER values.

The BER performance of the Digital FM Demodulator/discriminator was also measured against frequency deviations of ± 3 KHz at the IF center frequency and displayed the same results.

5. IMPLEMENTATION

The Digital FM Discriminator/demodulator circuit is implemented in a $0.5 \mu\text{m}$ triple-metal standard digital CMOS technology. Total chip area is less than 1 mm^2 , with a gate count of 3K unit cells. Operating supply voltage is 3 V and total current consumption is less than 1 mA at an IF sampling frequency of 5.1225 MHz. The designed IC requires no analog circuitry or external components, and it has a power

consumption much lower than conventional architectures.

6. RESULTS AND CONCLUSIONS

The zero-cross detection scheme utilized in the proposed Digital FM Discriminator/demodulator architecture attained a BER vs SNR performance which is better than not only conventional non-coherent and coherent FM demodulation schemes but also Viterbi-coded ones. The BER performance further increases at low SNR values, making this system especially advantageous for noisy channels or low power transmission.

The designed FM discriminator/demodulator IC takes full advantage of digital design techniques providing a highly integrated solution on a single chip, without even requiring an A/D converter. A high BER performance is attained at low power and low cost, while providing reliable operation against temperature and device-dependent parameters.

If still lower power consumption is required, the operating frequency of the IC can be decreased at the expense of BER performance. On the other hand, BER performance can be further improved by including an additional narrowband low-pass filter at baseband, prior to offset cancellation. This filter would have negligible effect on the total power consumption due to its extremely low operating frequency and still less on total cost of the system.

7. REFERENCES

- [1] S. Haykin, "Analog and Digital Communications," John Wiley & Sons, Toronto, 1989
- [2] T.S.Rappaport, "Wireless Communications," Prentice Hall, New Jersey, 1996
- [3] T.Rahkonen, K.Kananen, J.Kostamovaara, "A Digital FM Demodulator Chip Based on Measurement of IF-Signal's Period," ESSCIRC'95 Proceedings, Lille, France, September 1995, pp. 102-105
- [4] H. Rhie, "Digital FM Demodulator Using Pulse Generators," US Patent No.5850161, Dec. 15, 1998

[5] "MX-COM Inc. MX589 GMSK Modem Application Note," MX-COM Inc., Winston-Salem, NC, 1998

[6] B. Canpolat, "Design and Simulation of an Adaptive MLSE Receiver for GSM System," M.S. Thesis in Electrical and Electronics Engineering, METU, Ankara, 1994, pp. 77-78